REMARKS

Summary of the Office Action

In the Office Action, the disclosure is objected to for a particular informality.

Claims 1-4 stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,201,573 (hereinafter "the '573 patent") in view of U.S. Patent No. 4,827,145 to Arques.

Summary of the Response to the Office Action

The Specification has been amended at the paragraph beginning at page 1, line 20 in response to the Examiner's comments in the Office Action. Further, Applicants submit a Terminal Disclaimer concurrently herewith.

Objection to the Disclosure

In the Office Action, the disclosure is objected to for a particular informality. In particular, the Office Action recommends that "pickupping" at page 1, line 21 be replaced with --picking up--. In response, Applicants have amended at the paragraph beginning at page 1, line 20 in response to the Examiner's comments in the Office Action by incorporating the Examiner's helpful suggested change. Accordingly, withdrawal of the objection to the disclosure is respectfully requested.

Double Patenting Rejection

Claims 1-4 stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of the '573 patent in view of Arques.

Applicants traverse the statements in the Office Action regarding obviousness at least because claim 1 specifically recites the combination of the recited integrator circuit 30 and the recited capacitor 51 within a variable capacity integrator circuit 50. This novel combination, which is neither shown nor suggested by the applied art, produces unexpected results that provide advantages and solve problems that are also neither recognized nor suggested in the applied art. In particular, because of this specific combination of components, as recited in claim 1 of the instant application, the capacitor 51 is able to function so that a change of the voltage signal inputted to the capacitor is inputted to the amplifier. Accordingly, the electric charge corresponding to the change of the voltage signal and the capacity value of the variable capacity part flows into the variable capacity part. As a result, an integrated signal having a value corresponding to the change of the voltage signal inputted to the capacitor is outputted from the variable capacity integrator circuit to result in improvements in the overall solid state imaging device, as compared to prior arrangements. In particular, the solid state imaging device of the instant application has an improved signal-to-noise ratio, improved offset error yields, and has a small circuit scale. See, for example, page 3, lines 5-9 of the instant application's specification.

Moreover, Applicants respectfully traverse the rejection of dependent claims 2-4. In particular, the Office Action merely states at page 4, section 6 that the dependent claims "are rejected as being dependent on previously rejected claim 1 as discussed above." Applicants respectfully submit that such a rejection is improper as each of dependent claims 2-4 recites additional features to the solid-state imaging device combination recited in claim 1. Accordingly, the Office Action provides no explanation as to how such additional features are either shown or suggested by the applied art.

While Applicants traverse the double patenting rejections for at least the foregoing

reasons, Applicants also submit a Terminal Disclaimer concurrently herewith to facilitate allowance of the present application, thereby obviating the double patenting rejections.

Accordingly, Applicants respectfully request that the double patenting rejections of claims 1-4 be withdrawn. No additional rejections or objections remain in this application. Accordingly, Applicants respectfully request that the application be passed to issuance.

Information Disclosure Statement Issues

Applicants now refer to the JP-H09-051476-A publication which was cited in previously-submitted Information Disclosure Statements in this application on November 29, 2000 and July 11, 2002, and which was previously considered by the Examiner as indicated by the corresponding initialed PTO Form 1449's. Applicants note that this JP-H09-051476-A publication is a JP counterpart of the applied '573 patent. For the convenience of the Examiner, a complete English-language translation of the JP-H09-051476-A publication is concurrently being filed in an Information Disclosure Statement.

CONCLUSION

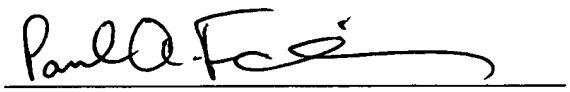
In view of the foregoing, Applicants respectfully request reconsideration and the timely allowance of the pending claims. Should the Examiner feel that there are any issues outstanding after consideration of this response, the Examiner is invited to contact Applicants' undersigned representative to expedite prosecution.

EXCEPT for issue fees payable under 37 C.F.R. § 1.18, the Commissioner is hereby authorized by this paper to charge any additional fees during the entire pendency of this application including fees due under 37 C.F.R. §§ 1.16 and 1.17 which may be required,

including any required extension of time fees, or credit any overpayment to Deposit Account 50-0310. This paragraph is intended to be a **CONSTRUCTIVE PETITION FOR EXTENSION OF TIME** in accordance with 37 C.F.R. § 1.136(a)(3).

Respectfully submitted,

MORGAN, LEWIS & BOCKIUS LLP

Dated: August 2, 2004 By: 

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